IN THE CLAIMS:

Listing of claims:

1-23 (canceled)

24. (previously presented) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate; and

wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, wherein the at least three insulation layers of the third voltage type transistor are identical in composition to the at least three insulation layers of the intermediate insulation layer of the non-volatile memory transistor.

25. (canceled)

26. (previously presented) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate;

wherein the first voltage-type transistor has a gate insulation layer having a thickness that is less than that of the second voltage-type transistor, and the second voltage-type transistor has a gate insulation layer having a thickness that is less than that of the third voltage type transistor; and

wherein the non-volatile memory transistor intermediate insulation layer has a thickness that is identical to that of the gate insulation layer of the third voltage-type transistor.

27. (previously presented) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third

voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate;

wherein the first voltage-type transistor has a gate insulation layer having a thickness that is less than that of the second voltage-type transistor, and the second voltage-type transistor has a gate insulation layer having a thickness that is less than that of the third voltage type transistor; and

wherein the first voltage-type transistor is positioned adjacent to the non-volatile memory transistor, the second voltage-type transistor is positioned adjacent to the first voltage-type transistor, and the third voltage-type transistor is positioned adjacent to the second voltage-type transistor, wherein the first voltage type transistor is positioned between the second voltage type transistor and the non-volatile memory transistor, and wherein the second voltage-type transistor is positioned between the third voltage-type transistor and the first voltage-type transistor.

28. (canceled)

29. (previously presented) A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers;

wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate;

wherein the first voltage-type transistor operates at a lower voltage range than that of the second voltage-type transistor, and the second voltage-type transistor operates at a lower voltage range than that of the third voltage-type transistor; and

wherein the first voltage-type transistor is positioned adjacent to the non-volatile memory transistor, the second voltage-type transistor is positioned adjacent to the first voltage-type transistor, and the third voltage-type transistor is positioned adjacent to the second voltage-type transistor, wherein the first voltage type transistor is positioned between the second voltage type transistor and the non-volatile memory transistor, and wherein the second voltage-type transistor is positioned between the third voltage-type transistor and the first voltage-type transistor.

30. (currently amended) A semiconductor device as in claim 24, ~~22,~~ wherein

the first voltage-type transistor includes a gate insulation ~~dielectric~~ layer having a first thickness,

the second voltage-type transistor includes the gate insulation ~~dielectric~~ layer formed from at least two insulation layers, the gate insulation ~~dielectric~~ layer of the second voltage-type transistor having a second thickness, and

the third voltage-type transistor includes ~~a~~ the gate insulation ~~dielectric~~ layer formed from at least three insulation layers, the gate insulation layer of the third voltage-type transistor having a third thickness, wherein the second thickness is greater than the first thickness and the third thickness is greater than the second thickness.

31. (new) A semiconductor device according to claim 24, wherein:

the first voltage-type transistor includes a gate insulation layer having a thickness of 3 – 13 nm,

the gate insulation layer of the second voltage-type transistor has a thickness of 4 – 15 nm, and

the gate insulation layer of third voltage-type transistor has a thickness of 16 – 45 nm.

32. (new) A semiconductor device according to claim 31, wherein the intermediate insulation layer of the non-volatile memory transistor has a thickness of 16 – 45 nm.

33. (new) A semiconductor device according to claim 24, wherein the gate insulation layer of the third voltage-type transistor has a thickness that is equal to that of the intermediate insulation layer of the non-volatile memory transistor.

34. (new) A semiconductor device according to claim 24, further comprising a selective oxidation layer on an upper surface of the floating gate, wherein the intermediate insulation layer of the non-volatile memory transistor extends over a portion of the selective oxidation layer.

35. (new) A semiconductor device according to claim 24, wherein the first voltage-type transistor is included in at least one circuit selected from a group consisting of a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder, an address buffer and a control circuit.

36. (new) A semiconductor device according to claim 24, wherein the second voltage-type transistor is included in at least one circuit selected from a group consisting of a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder and an interface circuit.

37. (new) A semiconductor device according to claim 24, wherein the third voltage-type transistor is included in at least one circuit selected from a group consisting of a voltage generation circuit, an erase voltage generation circuit and a step-up voltage circuit.

38. (new) A semiconductor device as in claim 24, wherein the first voltage level that operates the first voltage-type transistor is in a range of 1.8 – 3.3 V, the second voltage level that operates the second voltage-type transistor is in a range of 2.5 – 5 V, and the third voltage level that operates the third voltage-type transistor is in a range of 10 – 15 V.

39. (new) A semiconductor device according to claim 24, wherein the gate insulation layer of the third voltage-type transistor is formed from three insulation layers, including a lower layer having a thickness of 5 – 15 nm, a middle layer, and an upper layer having a thickness of 1 – 10 nm.

40. A semiconductor device according to claim 26, further comprising a selective oxidation layer on an upper surface of the floating gate, wherein the intermediate insulation layer of the non-volatile memory transistor extends over a portion of the selective oxidation layer.

41. (new) A semiconductor device according to claim 40, wherein:

the gate insulation layer of the second voltage-type transistor has a thickness of 4 – 15 nm, and

the gate insulation layer of third voltage-type transistor has a thickness of 16 – 45 nm.

42. (new) A semiconductor device as in claim 40, wherein the second voltage level that operates the second voltage-type transistor is in a range of 2.5 – 5 V, and the third voltage level that operates the third voltage-type transistor is in a range of 10 – 15 V.

43. (new) A semiconductor device according to claim 40, wherein the gate insulation layer of the third voltage-type transistor is formed from three insulation layers, including a lower layer having a thickness of 5 – 15 nm, a middle layer, and an upper layer having a thickness of 1 – 10 nm.

44. (new) A semiconductor device according to claim 27, further comprising a selective oxidation layer on an upper surface of the floating gate, wherein the intermediate insulation layer of the non-volatile memory transistor extends over a portion of the selective oxidation layer.

45. (new) A semiconductor device according to claim 27, wherein:

the gate insulation layer of the second voltage-type transistor has a thickness of 4 – 15 nm, and

the gate insulation layer of third voltage-type transistor has a thickness of 16 – 45 nm.

46. (new) A semiconductor device as in claim 27, wherein the second voltage level that operates the second voltage-type transistor is in a range of 2.5 – 5 V, and the third voltage level that operates the third voltage-type transistor is in a range of 10 – 15 V.

47. (new) A semiconductor device according to claim 27, wherein the gate insulation layer of the third voltage-type transistor is formed from three insulation layers, including a lower layer having a thickness of 5 – 15 nm, a middle layer, and an upper layer having a thickness of 1 – 10 nm.

48. (new) A semiconductor device according to claim 29, further comprising a selective oxidation layer on an upper surface of the floating gate, wherein the intermediate insulation layer of the non-volatile memory transistor extends over a portion of the selective oxidation layer.

49. (new) A semiconductor device according to claim 48, wherein:

the gate insulation layer of the second voltage-type transistor has a thickness of 4 – 15 nm, and

the gate insulation layer of third voltage-type transistor has a thickness of 16 – 45 nm.

50. (new) A semiconductor device as in claim 48, wherein the second voltage level that operates the second voltage-type transistor is in a range of 2.5 – 5 V, and the third voltage level that operates the third voltage-type transistor is in a range of 10 – 15 V.

51. (new) A semiconductor device according to claim 48, wherein the gate insulation layer of the third voltage-type transistor is formed from three insulation layers, including a lower layer having a thickness of 5 – 15 nm, a middle layer, and an upper layer having a thickness of 1 – 10 nm.

52. (new) A semiconductor device comprising a memory region, first, second and third transistor regions including field effect transistors,

the memory region including a split-gate non-volatile memory transistor comprising a source, a drain, a gate insulation layer, a floating gate formed on the gate insulation layer, a selective oxide insulation layer formed on the floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, wherein a portion of the intermediate insulation layer extends on the selective oxide insulation layer, and a control gate formed on the intermediate insulation layer, wherein the intermediate insulation layer is formed from at least three insulation layers,

the first transistor region including a first voltage-type transistor that operates at a first voltage range,

the second transistor region including a second voltage-type transistor that operates at a second voltage range, and

the third transistor region including a third voltage-type transistor that operates at a third voltage range that is higher than the first and second voltage levels,

wherein the third voltage-type transistor includes a gate insulation layer formed from at least three insulation layers, wherein the at least three insulation layers of the third voltage type transistor are identical in composition to the at least three insulation layers of the intermediate insulation layer of the non-volatile memory transistor.

53. (new) A semiconductor device according to claim 52, wherein the at least three insulation layers of the third voltage type transistor include upper and lower thermally oxidized layers separated from one another by another insulating layer.

54. (new) A semiconductor device according to claim 53, wherein the upper thermally oxidized layer comprises silicon oxide, the lower thermally oxidized layer comprises silicon oxide, and the insulating layer separating the upper and lower thermally oxidized layers from one another comprises silicon oxide.